ABSTRACT

A new method is provided for forming salicided surfaces to a FET device. Gate electrodes are formed, consisting, for the first embodiment of the invention, of stacked layers of silicon oxide (pad oxide), polysilicon and boronitride (BN). A thin layer of Ti/TiN is deposited, a low temperature anneal is performed. A selective wet etch removes unreacted Ti/TiN, a thin layer of silicon oxide is deposited. A thick layer of photoresist is deposited. The layer of photoresist is polished, stopping on the layer of BN. The surface of the layer of BN is now exposed, the layer of BN is removed. A thick layer of Ti/TiN is next deposited, filling the opening from where the layer of BN has been removed. A low temperature anneal anneals the layer of Ti/TiN, forming $TiSi_x$. The unreacted Ti/TiN is removed with a selective wet etch, leaving the layer of thick $TiSi_x$ in place overlying the gate electrode. A high temperature anneal is applied to reduce the sheet resistance of the layer of $TiSi_x$. As an alternate approach to the above cited sequence, forming the second embodiment of the invention, the function of the layer of photoresist can be replaced with a layer of boro-phosphate-silicate-glass (BPSG), the function of the top layer of BN can be replaced with a layer of silicon nitride.